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Presented for filing is a new divisional patent application of:

Applicant: HISASHI OHTANI

Title: MANUFACTURING METHOD OF SEMICONDUCTOR AND
MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

The prior application is assigned of record to Semiconductor Energy Laboratory Co., Ltd., a Japanese corporation, by virtue of an assignment submitted to the Patent and Trademark Office for recording on February 10, 1998 at Reel 8987 and Frame 0847.

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

Pages

| | |
|---------------|----------------------|
| Specification | 19 |
| Claims | 1 |
| Abstract | 1 |
| Declaration | 3 (copy from parent) |
| Drawing(s) | 6 |

CERTIFICATE OF MAILING BY EXPRESS MAIL

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Enclosures:

- Rule 63 declaration, copy from a previous application under rule 63(d) for continuation or divisional only.
- Information Disclosure Statement: Applicant calls attention to documents listed on attached form(s) PTO-892 and PTO-1449 from parent case(s). Per Rule 97(d) copies of those documents are not provided.
- Postcard.

This application is a divisional (and claims the benefit of priority under 35 USC §120) of U.S. application serial no. 09/021,639, filed February 10, 1998. The disclosure of the prior application is considered part of (and is incorporated by reference in) the disclosure of this application.

Preliminary Amendment:

Page 1 of the specification, before line 1, insert --This is a divisional of U.S. application serial no. 09/021,639, filed February 10, 1998, (allowed).--

Priority is claimed under 35 USC §119 based on priority application serial number 09-41540, filed February 10, 1997, in Japan.

1 total claims; 1 independent

| | |
|--|-------|
| Basic filing fee | \$690 |
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| Independent claims in excess of 3 times \$78 | \$0 |
| Fee for multiple dependent claims | \$0 |
| Total filing fee: | \$690 |

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

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Respectfully submitted,


Scott C. Harris
Reg. No. 32,030

Enclosures
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APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: MANUFACTURING METHOD OF SEMICONDUCTOR
AND MANUFACTURING METHOD OF
SEMICONDUCTOR DEVICE

APPLICANT: HISASHI OHTANI

CERTIFICATE OF MAILING BY EXPRESS MAIL

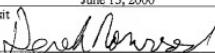
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MANUFACTURING METHOD OF SEMICONDUCTOR AND
MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

5

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of forming a semiconductor film comprising silicon or silicon compound having crystallinity over an insulating surface.

10 2. Description of the Related Art

A conventional technique is known in which a silicon film is formed over a glass or quartz substrate and a thin-film transistor (hereinafter referred to as "TFT") is formed by using the thus-formed silicon film.

15 The TFT is mainly used in the active matrix liquid crystal display device. The TFT is generally classified into the TFT using an amorphous silicon film and the TFT using a crystalline silicon film.

At present, the TFT using an amorphous silicon film is the mainstream. However, the TFT using an amorphous silicon film is low 20 in operation speed and hence its applicability is limited for purposes of reducing the size of a displayed image and displaying a high-speed moving picture.

Further, it is also attempted to constitute, by using TFTs, various circuits that are conventionally implemented as ICs. In this case, the 25 operation speed of the TFT using an amorphous silicon film is much

lower than a required value.

In view of the above, the TFT using a crystalline silicon film which is expected to operate at higher speed is now being studied extensively.

5 Among well known methods for obtaining a crystalline silicon film are:

- (1) forming a crystalline silicon film directly by CVD or the like;
- (2) crystallizing an amorphous silicon film by a heat treatment;
- (3) crystallizing an amorphous silicon film by irradiating it with 10 laser light; and
- (4) crystallizing an amorphous silicon film by irradiating it with strong light such as infrared light.

Among the above methods, methods (2)-(4) are mainly used.

Although method (2) is advantageous in that it can easily provide 15 a large-area film, the heat treatment temperature should be high and the quality of a resulting film is insufficient.

Although method (3) is advantageous in that thermal damage does not reach a glass substrate and a film having superior crystallinity can be obtained, it is difficult for method (3) to provide a 20 large-area film and the reproducibility of a process is low.

Although method (4) can easily provide a large-area film, the quality of a resulting film is insufficient.

Studies of the present inventors revealed that the crystallization of an amorphous film can be accelerated by using a metal element 25 typified by nickel (refer to Japanese Unexamined Patent Publication

Nos. Hei. 6-232059 and Hei. 7-321339).

By combining the crystallization technique using a metal element with methods (2)-(4), a crystalline silicon film can be obtained that has such high film quality as could not be obtained so far.

5 However, the crystallinity thus obtained is still insufficient as compared to that of a single crystal silicon wafer and the characteristics of a resulting TFT are far lower than those of a currently available insulated-gate field-effect transistor that constitutes an IC. In particular, there is a serious problem that
10 variations in device characteristics are large.

This is because grain boundaries exist in an uncontrollable state in a crystalline silicon film, i.e., in the channel of a TFT. In particular, since the grain boundaries extending direction cannot be controlled, the device characteristics vary to a large extent due to differences in
15 extending directions of grain boundaries existing in the channels, which necessarily occur when a large number of devices are formed.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a technique for obtaining a crystalline silicon film that can provide superior TFT
20 characteristics on a substrate having an insulating surface.

According to one aspect of the invention, there is provided a method for crystallizing at least part of an amorphous film made of silicon or a silicon compound by using a metal element for accelerating crystallization, comprising the steps of introducing the
25 metal element into part of the amorphous film; and forming a

temperature gradient in the amorphous film and causing crystal growth from a region where the metal element is introduced to another region by utilizing the temperature gradient.

According to another aspect of the invention, there is provided a method for crystallizing at least part of an amorphous film made of silicon or a silicon compound by using a metal element for accelerating crystallization, comprising the steps of introducing the metal element into part of the amorphous film; and forming a temperature gradient in the amorphous film in a direction extending from a region where the metal element is introduced to another region and causing crystal growth in the temperature gradient direction.

According to a further aspect of the invention, there is provided a method for crystallizing at least part of an amorphous film made of silicon or a silicon compound by using a metal element for accelerating crystallization, comprising the steps of introducing the metal element into part of the amorphous film; and causing the metal element to diffuse in a predetermined direction by utilizing the temperature gradient and causing crystal growth to proceed selectively in the predetermined direction.

In each of the three aspects of the invention, it is preferable to move the temperature gradient in the direction of the crystal growth, to thereby facilitate crystal growth in a direction parallel with the amorphous film.

Crystal growth in a direction parallel with the amorphous film

can be facilitated by moving the temperature gradient in the direction of the crystal growth at a speed corresponding to the rate of the crystal growth. This is particularly effective in obtaining a long crystal growth direction.

5 It is simple and convenient to form the temperature gradient by irradiation with linear infrared light. A means for instantaneously melting and solidifying a surface portion of a silicon film, such as a means using ultraviolet pulse laser light, cannot be used because actually it does not form a temperature gradient.

10 From the viewpoint of reproducibility and effects, it is preferable to use nickel as the metal element for accelerating the crystallization.

The metal element may be one or a plurality of elements selected from Fe, Co, Ni, Cu, Ru, Rh, Pd, Os, Ir, Pt, and Au.

BRIEF DESCRIPTION OF THE DRAWINGS

15 Figs. 1A-1C show a step of obtaining a crystalline silicon film according to a first embodiment of the present invention;

Figs. 2A-2E shows a manufacturing process of a TFT (thin-film transistor) according to the first embodiment;

Fig. 3 is a perspective view corresponding to Fig. 1A;

20 Fig. 4 is a perspective view corresponding to Fig. 1B;

Figs. 5A-5F schematically show various apparatuses according to a tenth embodiment of the invention; and

Figs. 6A and 6B shows a step of obtaining a crystalline silicon film according to a second embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

To practice the invention, it is important to form a negative temperature gradient in the direction of crystal growth that is performed by utilizing a metal element.

A specific example for realizing the above concept will be described below with reference to Figs. 1A-1B (sectional views) and Fig. 4 (perspective view).

First, as shown in Fig. 1A, the nickel element is provided selectively adjacent to the surface of an amorphous silicon film 102, i.e., adjacent to a part of the surface of the amorphous silicon film (the region of an opening 104). The region where the nickel element is introduced has a linear shape that is long in the direction perpendicular to the paper surface.

Then, linear infrared light emitted from each of linear infrared lamps 107 is reflected by each of reflecting plates 106, whereby the amorphous silicon film 102 is irradiated with linear infrared light beams while being scanned in a direction 100. The longitudinal direction of the linear beams is set coincident with that of the opening 104 (i.e., the extending direction of the nickel introduction region).

The infrared light is absorbed by the silicon film 102 mainly as thermal energy, whereby a temperature gradient shown in Fig. 1C is formed. The temperature gradient formed in the silicon film 102 moves as the lamp 107 is moved in the direction 100.

The direction (indicated by numeral 10 in Fig. 1B and 1C) of the negative temperature gradient is set coincident with the lamp movement direction 100 and the direction (indicated by numeral 108

in Fig. 1B) of the intended crystal growth.

In the above manner, the crystal growth can be performed in the direction 108 parallel with a substrate 101 uniformly over a long distance.

5 Crystal growth proceeds in the direction 108 parallel with the substrate 101 by merely performing a heat treatment in a heating furnace without conducting lamp irradiation.

In the invention disclosed in the specification, it is important to set the direction of the temperature gradient caused by the lamp 10 irradiation and the lamp movement direction coincident with the direction of crystal growth that proceeds by the heat treatment.

This is meaningful in the following points.

15 In the crystallization technique utilizing a metal element, crystallization proceeds as the metal element diffuses from a particular region (in the case of Figs. 1A and 1B, the opening 104 is formed) to other regions in the silicon film.

As in the case of impurities diffusion in a semiconductor, the metal element diffuses, with priority, from a region that is high in energy state to a region that is low in energy state.

20 Since the crystallization using the metal element proceeds in association with the diffusion of the metal element, forcing the diffusion of the metal element leads to control of the crystal growth.

That is, by forming a negative temperature gradient in a direction which coincides with the direction of intended crystal 25 growth, the metal element can be diffused intentionally in such a

direction. Intentionally making the diffusion direction of the metal element coincide with a certain direction means intentional acceleration of crystal growth in such a direction.

In this manner, crystal growth can be accelerated in a particular
5 direction.

It is also important to set the temperature gradient movement speed (specifically the lamp movement speed) in accordance with the crystal growth rate. This is to cause uniform crystal growth over a long distance gradually (the movement is performed in a step-like
10 10 manner depending on the crystal growth states) so as to keep the states of the crystal growth (including the temperature gradient state in the silicon film).

Further, where crystal growth is performed by forming a temperature gradient as shown in Figs. 1B and 1C, a phenomenon can
15 be restrained that the crystallization without utilizing the action of the metal element obstructs the crystal growth that is caused by utilizing the metal element so as to proceed parallel with the substrate 101.

The crystal growth parallel with the substrate 101 that is caused by utilizing the action of the metal element is stopped in a region
20 where the ordinary crystallization (in general, crystal growth proceeds in an amorphous silicon film by applying energy to it) proceeds that is not caused by utilizing the action of the metal element. This is a factor of reducing the crystal growth length in the direction 108.

25 According to the invention, by forming a negative temperature

gradient, it is possible to reduce the energy to be applied to a region where crystal growth with a metal element is intended. Accordingly, it is possible to avoid the above inconvenience.

In a region where crystal growth has been performed by the above method, crystal growth directions are well equalized and extending directions of grain boundaries well coincide with those crystal growth directions. Further, intervals between grain boundaries can be made approximately equal to each other.

When a number of TFTs are formed by utilizing the above crystal structure, the form of existence of crystal boundaries in the channel region can be made uniform among the TFTs. As a result, variations in characteristics among the TFTs can be restrained.

Embodiment 1

Figs. 1A-1C and 2A-2E show a manufacturing method according to this embodiment. First, as shown in Fig. 1A, a 500-Å-thick amorphous silicon film 102 is formed on a quartz substrate 101 by low-pressure thermal CVD.

Then, a 700-Å-thick silicon oxide film (not shown) is formed by plasma CVD and an opening 104 is formed therein to form a mask 103. The opening 104 is formed so as to have a linear shape (slit shape) extending perpendicularly to the paper surface of Figs. 1A and 1B.

Fig. 3 is a perspective view corresponding to Fig. 1A. To describe the structure in a simplified manner, Fig. 3 is drawn in such a manner that the opening 104 reaches two sidelines of the substrate. However,

in practicing the invention, the opening 104 need not always have such a shape.

Next, a nickel acetate salt solution containing the nickel element at 10 ppm (in terms of weight) is applied and an excess of the solution 5 is removed with a spin coater. In this state, the nickel element is held in contact with the surface as indicated by numeral 105 in Fig. 1A.

The state of Fig. 1A is thus obtained.

Then, annealing is performed by using a linear lamp annealing apparatus. The lamp annealing apparatus is so configured as to 10 enable irradiation with linear beams by causing infrared light that is emitted from each of long and narrow, rod-like lamps 107 to be reflected by each of reflecting plates 106 (see Figs. 1B and 4).

The positional relationship between the sample and the lamps 107 is such as to be shown in Fig. 4. The crystallization is performed 15 as follows:

(1) The longitudinal direction of the beams is set coincident with that of the opening 104.

(2) The linear infrared light beams are moved in the direction (indicated by numeral 100 in Fig. 1B) perpendicular to the linear 20 beams at a given speed starting from the opening 104 or a position close to it.

As a result, a region irradiated with the linear infrared light beams is heated to about 800°C in a short while. The nickel element is provided adjacent to (held in contact with) the surface of the 25 amorphous silicon film 102 in the region of the opening 104, and it

diffuses into the amorphous silicon film 102 as it is irradiated with the infrared light beams. Crystal growth proceeds in a direction 108 due to the action of the diffused nickel element and energy supplied by the infrared light beams.

5 It is preferred that the scanning speed of the infrared light beams be set equal to the crystal growth rate. The appropriate scanning speed of the infrared light beams needs to be determined by conducting a preliminary experiment because it depends on the thickness and the film quality of the amorphous silicon film 102, the 10 irradiation intensity and the spectrum of the infrared light beams, the heat capacity of the substrate 101, and other factors.

It is also important that a temperature gradient be formed in the silicon film so as to have a temperature profile as shown in Figs. 1B and 1C. The temperature profile (temperature gradient state) is 15 adjusted by changing the type and/or the positions of the reflecting plates 106 and the positions of the lamps 107.

The crystal growth proceeds perpendicularly to the longitudinal direction of the opening 104 in such a manner that growth directions are generally equal to each other.

20 Fig. 4 schematically shows a state that a region 400 has been crystallized by the irradiation and the scanning with the linear light beams emitted from the lamps 107. Crystal growth directions are indicated by numeral 108.

In the above manner, a crystalline silicon film 109 is obtained in 25 which the directions of the crystal growth that starts from the region

of the opening 104 are well equalized with the direction indicated by numeral 108 in Fig. 2A.

After the crystalline silicon film 109 is obtained, the silicon oxide film mask 103 is removed.

5 Then, the nickel element is removed from the film 109. Specifically, a 300-Å-thick thermal oxidation film is formed by performing a heat treatment at 950°C for 30 minutes in an oxygen atmosphere containing HCl at 3 volume percent. The nickel element is removed from the film 109 during this course.

10 In this step, the nickel element evaporates as nickel chloride and is thereby eliminated outside.

The thickness of the crystalline silicon film 109 decreases to 350 Å as a result of the formation of the thermal oxidation film.

Next, the thus-formed thermal oxidation film is removed. The 15 crystalline silicon film 109 is patterned into a pattern of become the active layer (indicated by numeral 110 in Fig. 2B) of a TFT.

A gate insulating film 111 is then formed. Specifically, a 500-Å-thick silicon oxide film is formed by plasma CVD and then a 200-Å-thick thermal oxidation film is formed. The thermal oxidation film is 20 formed inside the silicon oxide film that has been formed by CVD, i.e., on the surface of the active layer 110.

A 250-Å-thick active layer 110 and a 700-Å-thick gate insulating film 111 covering the active layer 110 are thus formed.

Thereafter, an aluminum film containing scandium at 0.18 wt% is 25 formed by sputtering and then patterned into a starting member of a

gate electrode.

The reason for having the aluminum film contain scandium is to prevent formation of protrusions called hillocks and whiskers in later steps.

5 An anodic oxide layer 113 (it is not appropriate to call this layer a film) and an anodic oxide film 114 are formed by performing anodization in the following manner with the gate electrode starting member used as the anode.

10 First, the porous anodic oxide layer 113 is formed by performing anodization in a state that a resist mask (not shown) that was used in patterning the aluminum film is left.

15 The anodic oxide film 114 that is dense in film quality is then formed by again performing anodization after removing the resist mask.

20 The growth lengths of the porous anodic oxide layer 113 and the dense anodic oxide film 114 are set at 400 nm and 80 nm, respectively.

An anodic oxide film can selectively be made porous or dense depending on the electrolyte used in the anodization.

25 The state of Fig. 2B is thus obtained. Subsequently, the exposed part of the silicon oxide film 111 is removed to leave a gate insulating film 115 (see Fig. 2C).

Then, after the porous anodic oxide layer 113 is removed, the active layer 110 is doped with P (phosphorus) by plasma doping. As a result, a source region 116, a drain region 120, low-concentration

impurity regions (high-resistivity regions) 117 and 119, and a channel forming region 118 are formed in a self-aligned manner (see Fig. 2D).

Subsequently, irradiation with laser light or infrared light is 5 performed to activate the dopant introduced in the above step and to repair damage of the doped regions through annealing.

Then, a silicon nitride film 121 and a polyimide resin film 122 are formed as an interlayer insulating film. After contact holes are 10 formed through the films 121 and 122, a source electrode 123 and a drain electrode 124 are formed. An n-channel thin-film transistor is thus completed (see Fig. 2E).

By employing the manufacturing process of this embodiment, a crystalline silicon film having superior crystallinity can be formed over a large area.

15 Embodiment 2

According to this embodiment, in the annealing step of the first embodiment that uses linear infrared light beams, auxiliary lamps are arranged in addition to the main lamps 107. The preliminary heating is performed on a region to be irradiated by the main lamps 107.

20 In this embodiment, auxiliary lamps 603 are disposed ahead of main lamps 601 as shown in Fig. 6A. Reflecting plates 602 are provided only for the main lamps 601, whereby a temperature gradient as shown in Fig. 6B is formed.

The crystal growth states can be changed by altering the shape of 25 the temperature gradient.

Embodiment 3

According to this embodiment, in the constitution of the first embodiment, a silicon film is scanned with linear infrared light beams by moving the substrate rather than the lamp system.

5 The relative movement relationship between the substrate and the lamp system in this embodiment is the same as in the first embodiment.

Embodiment 4

According to this embodiment, in the constitution of the first
10 embodiment, silicon or silicide is used to form the gate electrode of a TFT.

In this case, by virtue of high heat resistance of the gate electrode, the annealing to be performed after the impurity ion doping can be performed by a heat treatment.

Embodiment 5

According to this embodiment, in the constitution of the first embodiment, a TFT to be formed is of the bottom gate type structure.
A bottom gate type TFT has been put into practical use in such a manner as to use an amorphous silicon film. Therefore, there is an
20 advantage that a manufacturing process of this embodiment a manufacturing process of a bottom gate type TFT using an amorphous silicon film can be partially commonized.

Embodiment 6

According to this embodiment, a p-channel TFT and an n-channel
25 TFT are formed on the same substrate by using the crystallization

technique of this invention and a complementary circuit of those TFTs is formed.

In this embodiment, both of doping for imparting p-type conductivity and doping for imparting n-type conductivity need to be 5 performed to separately provide the two types of channels.

Embodiment 7

According to this embodiment, in the constitution of the first embodiment, a semiconductor film of a silicon compound represented by $\text{Si}_x\text{Ge}_{1-x}$ is used instead of a silicon film. The invention can also be 10 applied to a compound semiconductor containing silicon.

Embodiment 8

According to this embodiment, in the constitution of the first embodiment, a polysilicon substrate is used as the substrate.

The polysilicon substrate that is used for the solar battery cannot 15 be acquired at as low a price as the glass substrate.

In general, the polysilicon substrate is high in both impurity concentration and defect density and hence cannot be used as an IC substrate.

However, where the polysilicon substrate is used for forming a 20 TFT, its high impurity concentration and defect density are not serious problems.

In this embodiment, a silicon oxide film is formed on the surface of a polysilicon substrate by plasma CVD and a thermal oxidation film is formed thereon to provide an insulating surface. A TFT is formed 25 on the insulating surface by the method described in the first

embodiment.

Embodiment 9

According to this embodiment, in the constitution of the first embodiment, nickel is introduced by ion implantation. In this case,
5 the nickel introduction amount can be controlled precisely. Further, a resist material can be used to form the mask.

Embodiment 10

This embodiment is directed to examples of electronic apparatuses that use an integrated circuit constituted of TFTs. The
10 invention can be applied to a circuit constituted of TFTs that are formed on a substrate having a proper insulating surface. Figs. 5A-5F outline the respective apparatuses.

Fig. 5A shows a portable information processing terminal having a function of performing communication via telephone lines.

15 In this electronic apparatus, an integrated circuit 2006 that is a composite circuit according to the invention is incorporated in a main body 2001. The electronic circuit further has an active matrix liquid crystal display 2005, a camera section 2002 for capturing an image, and a manipulation switch 2004.

20 Fig. 5B shows an electronic apparatus called a head-mounted display, which has a function of virtually displaying, when mounted on a head, an image in front of the eyes. A main body 2101 is mounted on a head with a band 2103. An image is formed by liquid crystal display devices 2102 corresponding to the respective eyes.

25 Fig. 5C shows a car navigation apparatus. This electronic

apparatus has a function of displaying map information and other various kinds of information based on signals transmitted from an artificial satellite. Information transmitted from the satellite and received by an antenna 2204 is processed by electronic circuits 5 incorporated in a main body 2201 and necessary information is displayed on a liquid crystal display device 2202. The apparatus is manipulated through manipulation switches 2203.

Fig. 5D shows a cellular telephone. In this electronic apparatus, a main body 2301 is provided with an antenna 2306, a voice output 10 section 2302, a liquid crystal display device 2304, manipulation switches 2305, and a voice input section 2303.

An electronic apparatus shown in Fig. 5E is a portable imaging apparatus called a video camera. In this electronic apparatus, a main body 2401 has, on an opening/closing member, a liquid crystal display 15 2402 and manipulation switches 2404.

The main body 2401 is further provided with an image receiving section 2406, integrated circuits 2407, a sound input section 2403, manipulation switches 2404, and a battery 2405.

An electronic apparatus shown in Fig. 5F is a projection liquid 20 crystal display device. In this apparatus, a main body 2501 is provided with a light source 2502, a liquid crystal display device 2503, and an optical system 2504. This apparatus has a function of projecting an image onto a screen 2505.

The liquid crystal display device used in each of the above 25 electronic apparatuses may be of either a transmission type or a

reflection type. The transmission type is advantageous in terms of display characteristics while the reflection type is advantageous for the purpose of lowering the power consumption or reducing the size and weight.

5 Flat panel displays such as an active matrix EL display and a plasma display can be used as the display device.

By utilizing the invention, a crystalline silicon film that can provide superior TFT characteristics can be obtained on a substrate having an insulating surface.

10 In particular, by equalizing crystal growth directions, grain boundaries extending directions can also be made coincident with those crystal growth directions. This is very effective in equalizing device characteristics of a number of devices because the states of grain boundaries in the active layer of each device can be made uniform among those devices.

15 Such a crystalline silicon film can be used to form thin-film semiconductor devices such sensors and a diode in addition to a TFT.

WHAT IS CLAIMED IS:

1. A method for manufacturing semiconductor material comprising the steps of:

5 introducing a metal element into a region of an amorphous semiconductor film, the metal element accelerating crystallization of the semiconductor film;

crystallizing at least part of the semiconductor film by forming a temperature gradient in the semiconductor film and causing
10 crystal growth from the region where the metal element is introduced to another region of the semiconductor film by utilizing the temperature gradient.

ABSTRACT OF THE DISCLOSURE

The nickel element is provided selectively, i.e., adjacent to part of the surface of an amorphous silicon film in a long and narrow opening. The amorphous silicon film is irradiated with linear infrared light
5 beams emitted from respective linear infrared lamps while scanned with the linear beams perpendicularly to the longitudinal direction of the opening. The longitudinal direction of the linear beams are set coincident with that of the opening. The infrared light beams are absorbed by the silicon film mainly as thermal energy, whereby a
10 negative temperature gradient is formed in the silicon film. The temperature gradient moves as the lamps are moved for the scanning. The direction of the negative temperature gradient is set coincident with the lamp movement direction and an intended crystal growth direction, which enables crystal growth to proceed parallel with a
15 substrate uniformly over a long distance.

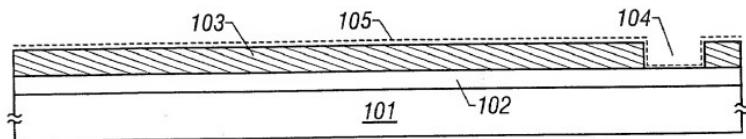


FIG. 1A

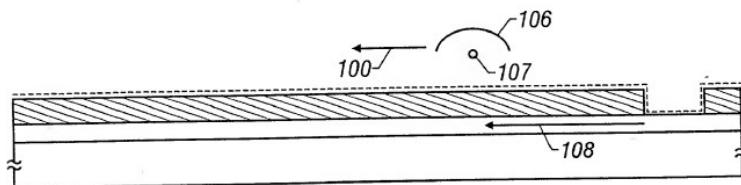


FIG. 1B

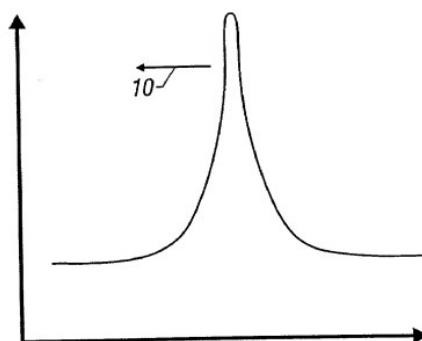


FIG. 1C

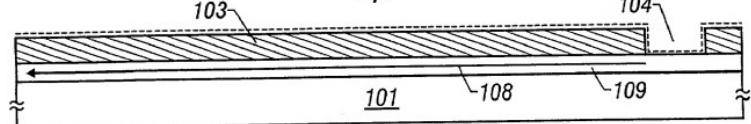


FIG. 2A

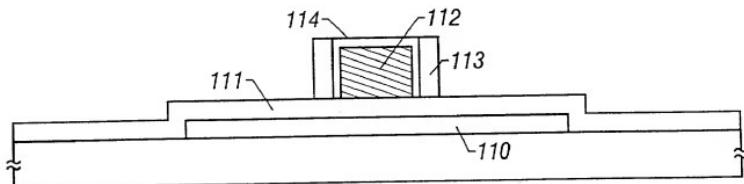


FIG. 2B

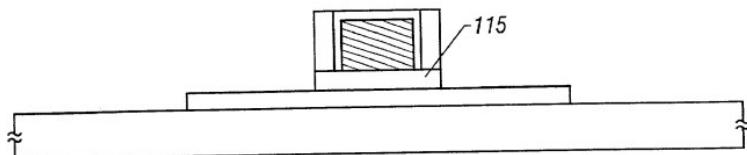


FIG. 2C

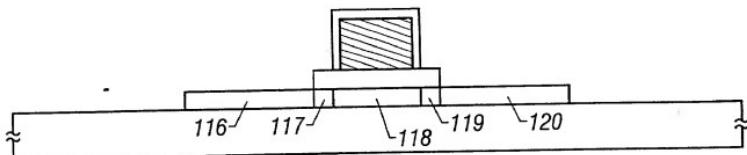


FIG. 2D

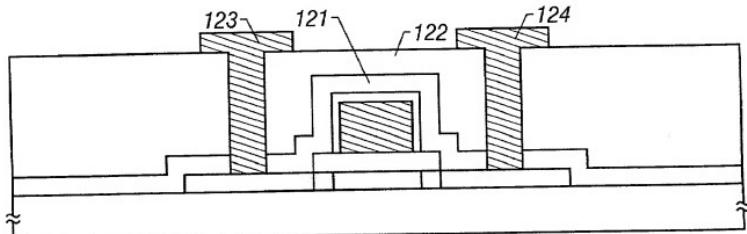


FIG. 2E

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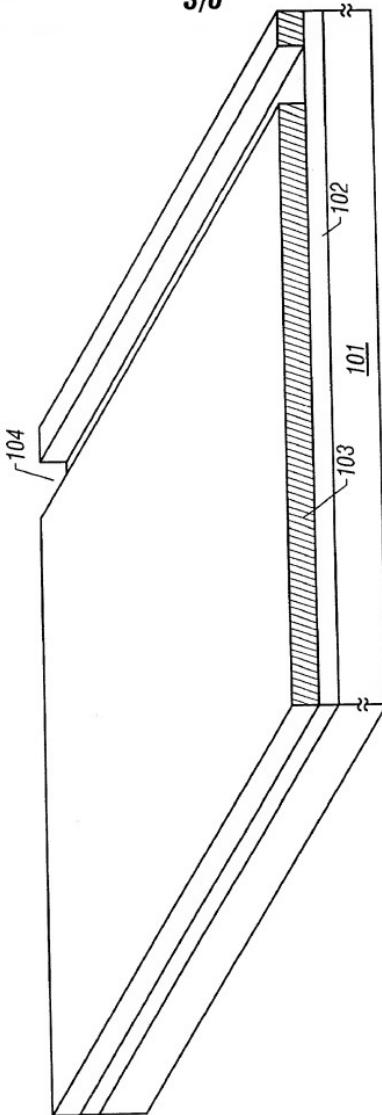


FIG. 3

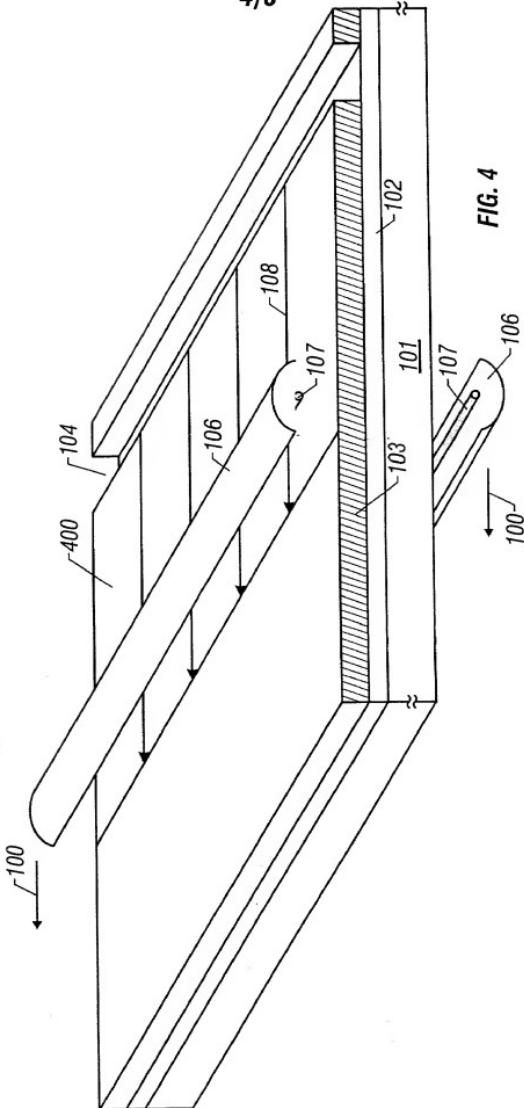
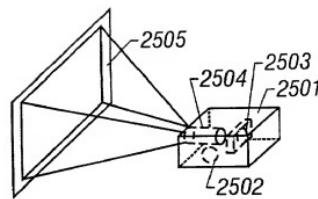
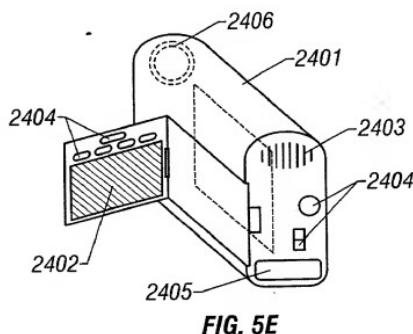
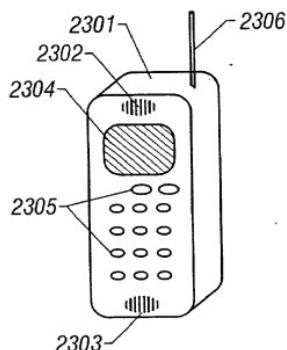
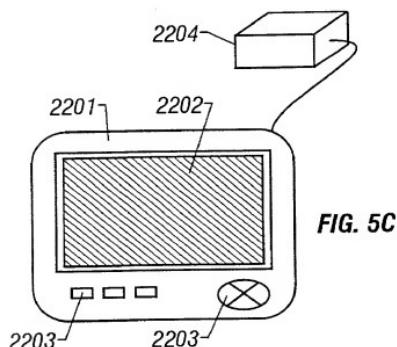
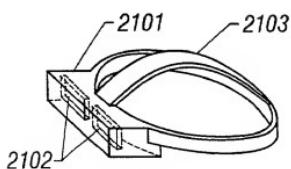
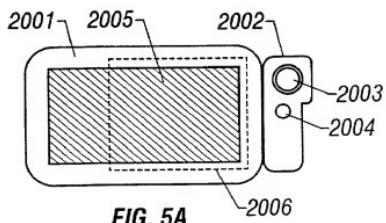


FIG. 4



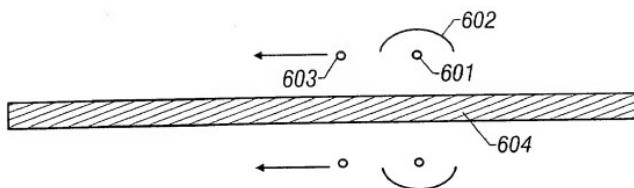


FIG. 6A

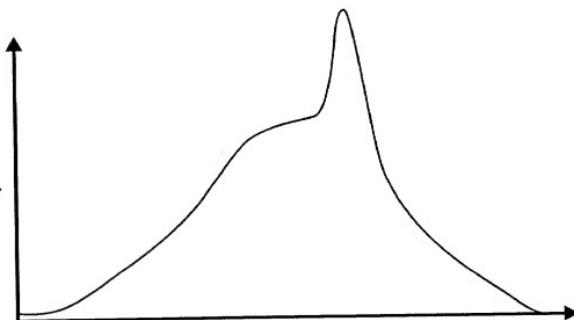


FIG. 6B

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名が発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している旨明確さについて、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

MANUFACTURING METHOD OF SEMICONDUCTOR
AND MANUFACTURING METHOD OF
SEMICONDUCTOR DEVICE

the specification of which is attached hereto unless the following box is checked:

二月日に提出され、米国出願番号または特許協定条約
国際出願番号を _____ とし。
(該当する場合) _____ に訂正されました。

was filed on _____
as United States Application Number or
PCT International Application Number
and was amended on

(if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1章5.6項に定義される
おり、特許実務の立場について重要な情報を開示する義務が
あることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編第119条(a)-(d)項又は365条(b)項に基き下記の、米国以外の国々少くとも一ヶ国を指定している特許出願を第365条(a)項に基づく提出日を除く。又は以下の特許出願もしくは発明者登録出願について米国外の提出権をここに主張するとともに、優先権を主張している。出願の前に出願された特許または発明者登録の外に出願を以下に、専門をマークすることで、示しています。

Prior Foreign Application(s)

外国出願番号

9-41540

(Number)
(番号)

Japan

(Country)
(国名)(Number)
(番号)(Country)
(国名)

私は、第35編米国法典第119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

(Application No.)
(出願番号)(Filing Date)
(出願日)

私は、下記の米国法典第35編第120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基く権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編第112条第1項又は特許協力条約で規定する方法で先行する米国特許出願に開示されていない限り、その後米国出願提出日以降で本出願の日本国内または特許協力条約国際出願提出日までの期間中に入手された、連邦規則法典第37編1条5.6項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

(Application No.)
(出願番号)(Filing Date)
(出願日)(Application No.)
(出願番号)(Filing Date)
(出願日)

私は、私自身の知識に基いて不真言まで私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基いて表明が全て真実であると信じてること、さらに故意になされた虚偽の表明及びそれと同様の行為は米国法典第18編第1001条に基き、罰金または刑務所、もしくはその両方により懲罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のことを宣言します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権を主張なし

February 10, 1997

(Day/Month/Year Filed)

(出願年月日)

(Day/Month/Year Filed)

(出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)
(出願番号)(Filing Date)
(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

(日本語宣言書)

著者様へ 本件で記載する第一の
二元をとるべき代理人として進行する手続はなされぬ
として、下記の者を名前としてます。(弁護士、または代理
の元よりはるかなる者を名前のこと)

Scott C. Harris Reg. No. 32,030

POWER OF ATTORNEY: As a named inventor, I hereby appoint
the following attorney(s) and/or agent(s) to prosecute this
application and transact all business in the Patent and Trademark
Office connected therewith (list name and registration number).

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Full name of sole or first inventor

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Inventor's signature

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第二共同発明者

Full name of second joint inventor, if any

発明者の署名

日付

Inventor's signature

Date

住所

Residence

国籍

Citizenship

私書箱

Post Office Address

(第三以降の共同発明者についても同様に記載し、署名をす
ること) (Supply similar information and signature for third and
subsequent joint inventors.)

- Please see attached page 3a for names, addresses and signatures of
additional inventors, if any.